MULTI-DIRECTIONAL TRENCHING OF A DIE IN MANUFACTURING SUPERJUNCTION DEVICES

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a divisional application of U.S. patent application Ser. No. 12/031,895, filed on Feb. 15, 2008, entitled "Multi-Directional Trenching in Manufacturing Superjunction Devices," currently pending, which claims priority to U.S. Provisional Patent Application No. 60/975,878, filed on Sep. 28, 2007, entitled "Multi-Directional Trenching in Manufacturing Superjunction Devices," the entire contents of all of which are incorporated by reference herein.

BACKGROUND OF THE INVENTION

An embodiment of the present invention relates generally to a method of manufacturing a semiconductor device, and more particularly, to a method of manufacturing a superjunction device with a first plurality of trenches having one orientation and a second plurality of trenches having a second orientation different than the first orientation.

Semiconductor wafer manufacture generally refers to the process of making integrated circuits on silicon wafers. A typical semiconductor wafer is generally circular in plan view. Individual electronic circuits or devices are formed across at least one surface of the wafer and then the wafer is typically cut (sawed or diced) into a plurality of individual "dies" for packaging into individual integrated circuits (ICs).

Since the invention of superjunction devices by Dr. Xingbi Chen, as disclosed in U.S. Pat. No. 5,216,275, the contents of which are incorporated by reference herein, there have been many attempts to expand and improve on the superjunction effect of his invention. U.S. Pat. Nos. 6,410,958, 6,300,171 and 6,307,246 are examples of such efforts and are incorporated herein by reference.

Trench type superjunction devices are expected to replace multi-epi superjunction devices because of the potential lower processing cost. FIG. **1**A illustrates a top plan view of a wafer **10** used in the manufacturing of a plurality of trench-type superjunction devices or dies **20**. FIG. **1**B shows a magnified view of two dies **20** representative of the plurality of dies **20** located on the wafer **10**. Each die **20** includes a plurality of trenches **22**, each of the trenches **22** traversing the die **20** in a generally horizontal orientation. FIG. **1**C shows an alternate configuration wherein the plurality of trenches **22** are each oriented generally vertically on the die **20**. In each case, all of the trenches **22** on all of the dies **20** of the wafer **10** have the same orientation. FIG. **1**D illustrates an enlarged partial cross-sectional view of a die **20** having a plurality of trenches **22** formed in a silicon layer **12** disposed on a substrate **11**. A plurality of corresponding mesas **24** are thereby formed, each mesa **24** being capped by a layer of oxide **26**. The trenches **22** are typically filled with a refill material **28**.

Generally, the cost of semiconductor device manufacturing has been reduced by condensing the design rules (recommended parameters) and enlarging the diameter of the process wafer. The design rules reduction may be applied to trench-type superjunction technology, as described in co-pending U.S. patent application Ser. No. 11/962,530. However, conventional trenching methods tend to cause wafer bowing and warping. Such deformations are especially

prevalent when trenching large diameter wafers (e.g., greater than about six inches). Once bowing and warping occurs, a wafer typically can no longer be processed effectively, if at all. Further, even if the wafer remains capable of processing, there is a higher risk of chipping or breakage. The degree of bowing and/or warping is greater when using deep trenching, such as the type of deep trenching used, for example, in the formation of superjunction devices. Thus, the use of conventional trenching methods for manufacturing superjunction devices does not permit the cost reduction achieved by increasing the diameter of the wafer.

It is desirable to provide a method of manufacturing trench-type superjunction devices that minimizes and/or eliminates the effects of bowing and warping. It is further desirable to provide a method of manufacturing trench-type superjunction devices that reduces manufacturing costs by enabling the use of larger wafer diameters.

BRIEF SUMMARY OF THE INVENTION

Briefly stated, embodiments of the present invention comprise a method of manufacturing a superjunction device. One embodiment of the method includes providing a semiconductor wafer having at least one die. The method further includes forming at least one first trench in the at least one die, the at least one first trench having a first orientation. The method also includes forming at least one second trench in the at least one die, the at least one second trench having a second orientation that is different from the first orientation. In preferred embodiments, at least one additional trench is formed in the at least one die, each additional trench having an orientation that is different from at least one of the first orientation and the second orientation.

Another embodiment of the present invention comprises a method of manufacturing a superjunction device. The method includes providing a semiconductor wafer having at least one die. The method further includes forming a first plurality of trenches in the at least one die, each of the first plurality of trenches having a first orientation. The method also includes forming a second plurality of trenches in the at least one die, each of the second plurality of trenches having a second orientation that is different from the first orientation.

Embodiments of the present invention also comprise superjunction devices. In one embodiment, the superjunction device includes a semiconductor wafer having at least one die. At least one first trench is formed in the at least one die, the at least one first trench having a first orientation. At least one second trench is formed in the at least one die, the at least one second trench having a second orientation that is different from the first orientation.

Yet another embodiment of the present invention comprises other types of semiconductor devices formed on or in a semiconductor wafer. The semiconductor wafer includes at least one die. At least one first trench is formed in the at least one die, the at least one first trench having a first orientation. At least one second trench is formed in the at least one die, the at least one second trench having a second orientation that is different from the first orientation.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing summary, as well as the following detailed description of preferred embodiments of the invention, will be better understood when read in conjunction with the appended drawings. For the purpose of illustration, there are shown in the drawings embodiments which are presently